



UNITED STATES PATENT AND TRADEMARK OFFICE

llm
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,388	12/07/2003	Paul M. Buxton	TAI.0800	4630
7590	02/02/2007	EXAMINER KHUU, HIEN DIEU THI		
Daniel J. Noblitt Noblitt & Gilmore, LLC Suite 6000 4800 North Scottsdale Road Scottsdale, AZ 85251		ART UNIT 2863	PAPER NUMBER	
		MAIL DATE 02/02/2007	DELIVERY MODE PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
---------------------------------	-------------	---	---------------------

10/730,388 12/7/03 Buxton

EXAMINER

Cindy Khur

ART UNIT PAPER

2863 20070123

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The information disclosure statement filed 12/22/2006 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. The followings are a list of NPLs require a legible copy: Tobin, "Automatic Classification of Spatial Signatures on Semiconductor Wafermaps"; Kameyama, "Semiconductor Defect Classification using Hyperellipsoid Clustering Neural Networks and Model Switching"; and Kamowski, "The Application of Spatial Signature Analysis to Electrical Test Data".

NPL document, "Mining IC test data to optimize VLSI testing" submitted 12/28/06 are now considered.


John Barlow
Supervisory Patent Examiner
Technology Center 2800

chk 1/23/07